NEC

MOS FIELD EFFECT TRANSISTOR
2SJ581

SWITCHING
P-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SJ581 is P-Channel DMOS Field Effect Transistor that features a low on-resistance and excellent switching characteristics, designed for high current switching applications such as DC to DC converter and load switch.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SJ581	MP-10

FEATURES

- Low on-state resistance :
  $R_{DS(on)1}$ = 70 mΩ TYP. (V_{GS} = –10 V, I_D = –6 A)
  $R_{DS(on)2}$ = 120 mΩ TYP. (V_{GS} = –4 V, I_D = –6 A)
- Low input capacitance :
  C_{iss} = 1210 pF TYP. (V_{DS} = –10 V, f = 1MHz)
- Narrow gate cut-off voltage width :
  $V_{GS(off)}$ = –1.0 to –2.0 V
- Built-in gate protection diode.
- Suitable to automatically assembling.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage	V_{DSS}	–60	V
Gate to Source Voltage	$V_{GSS(AC)}$	±20	V
Gate to Source Voltage	$V_{GSS(DC)}$	–20, 0	V
Drain Current (DC)	$I_{D(DC)}$	±12	A
Drain Current (pulse) **Note**	$I_{D(pulse)}$	±48	A
Total Power Dissipation (T_A = 25 °C)	P_T	1.8	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

Note PW ≤ 10 μs, Duty Cycle ≤ 1 %

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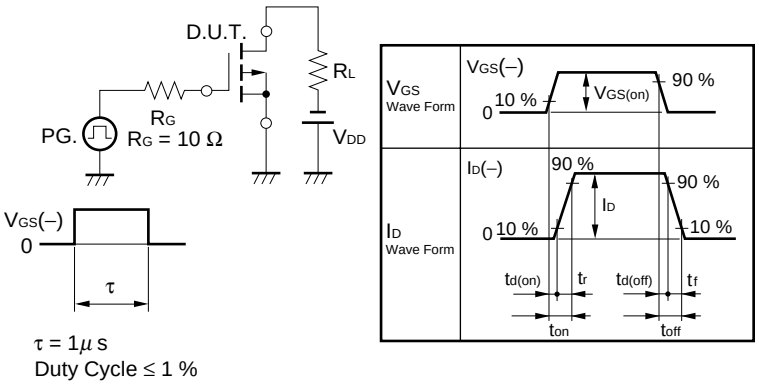
ELECTRICAL CHARACTERISTICS(T_A = 25°C)

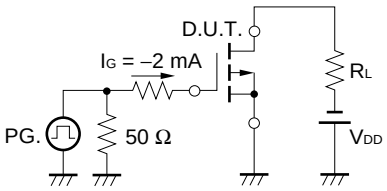
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	I_{DSS}	V_{DS} = –60 V, V_{GS} = 0 V			–10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1.0 mA	–1.0		–2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –6 A	5.0			S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –6 A		70	100	mΩ
	$R_{DS(on)2}$	V_{GS} = –4 V, I_D = –6 A		120	185	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V, V_{GS} = 0 V, f = 1 MHz		1210		pF
Output Capacitance	C_{oss}			520		pF
Reverse Transfer Capacitance	C_{rss}			180		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = –6 A, $V_{GS(on)}$ = –10 V,		15		ns
Rise Time	t_r	V_{DD} = –30 V,		130		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		95		ns
Fall Time	t_f			80		ns
Total Gate Charge	Q_G	I_D = –12 A, V_{DD} = –48 V,		42		nC
Gate to Source Charge	Q_{GS}	$V_{GS(on)}$ = –10 V		8.0		nC
Gate to Drain Charge	Q_{GD}			10		nC
Diode Forward Voltage	$V_{F(S-D)}$	I_F = –12 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = –12 A, V_{GS} = 0 V,		120		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		230		nC

TEST CIRCUIT 1 SWITCHING TIME



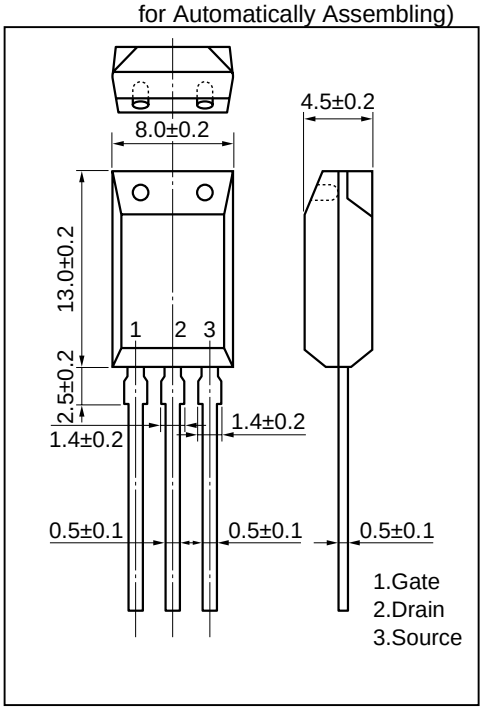
τ = 1μ s
Duty Cycle ≤ 1 %

TEST CIRCUIT 2 GATE CHARGE

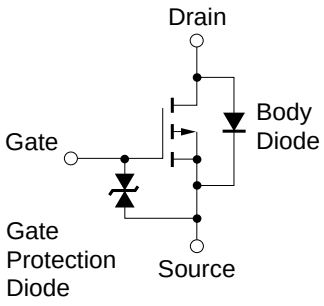


PACKAGE DRAWING (Unit : mm)

MP-10 (Isolated TO-220 class Package for Automatically Assembling)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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